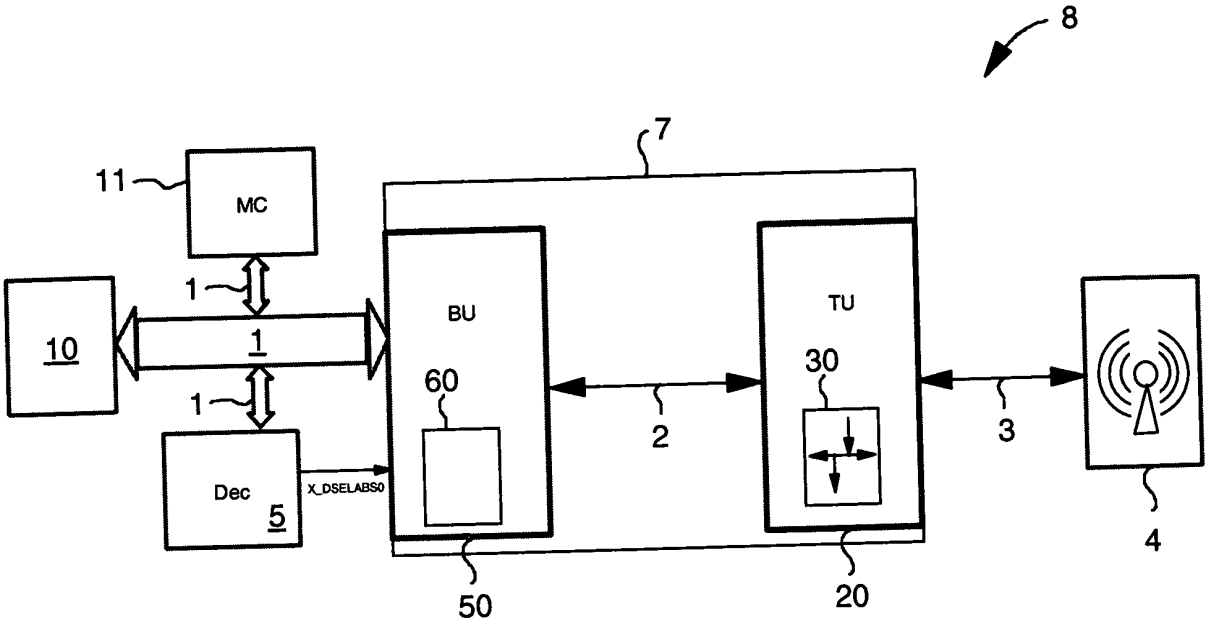
8
7
11
MC
1
10
1
1
Dec
5
X_DSELABS0
BU
60
50
2
TU
30
20
3
4

Fig. 1

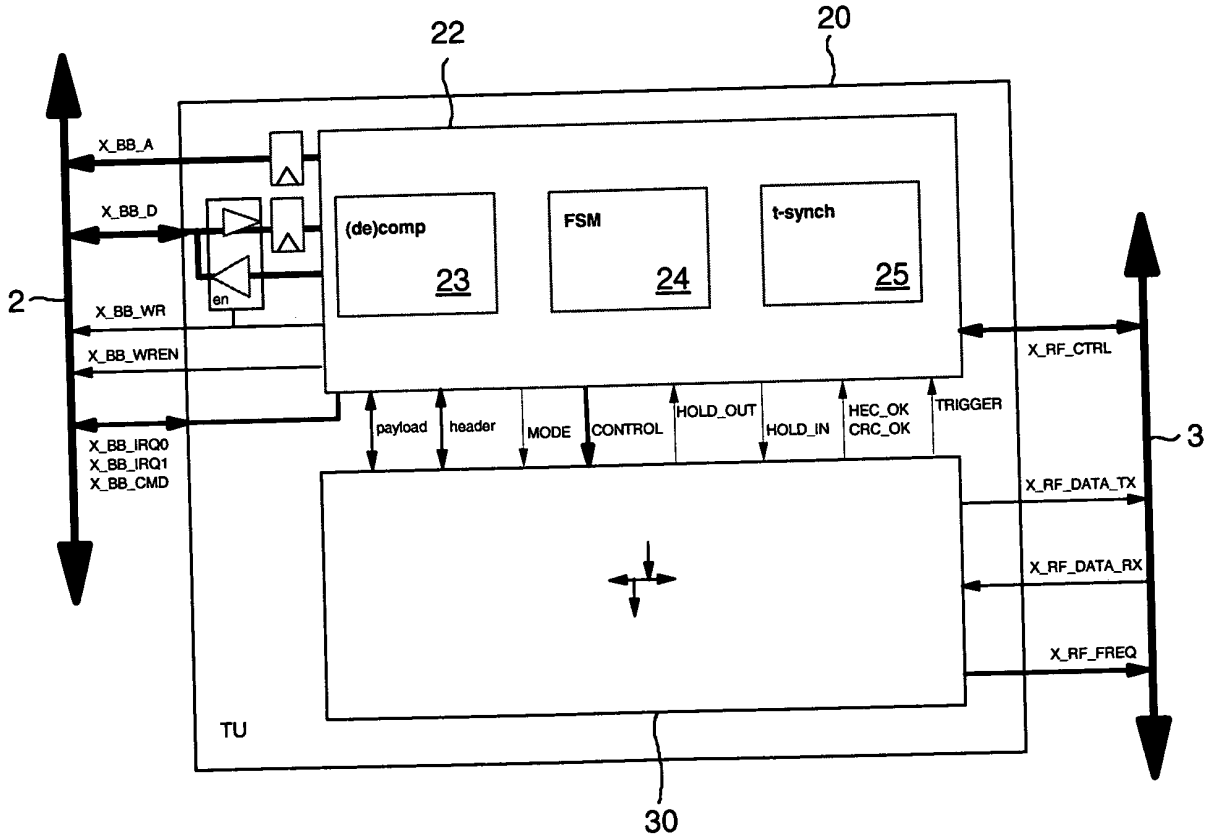
22
20
X_BB_A
X_BB_D
2
X_BB_WR
X_BB_WREN
X_BB_IRQ0
X_BB_IRQ1
X_BB_CMD
en
(de)comp
23
FSM
24
t-synch
25
payload
header
MODE
CONTROL
HOLD_OUT
HOLD_IN
HEC_OK
CRC_OK
TRIGGER
X_RF_CTRL
3
X_RF_DATA_TX
X_RF_DATA_RX
X_RF_FREQ
TU
30

Fig. 2

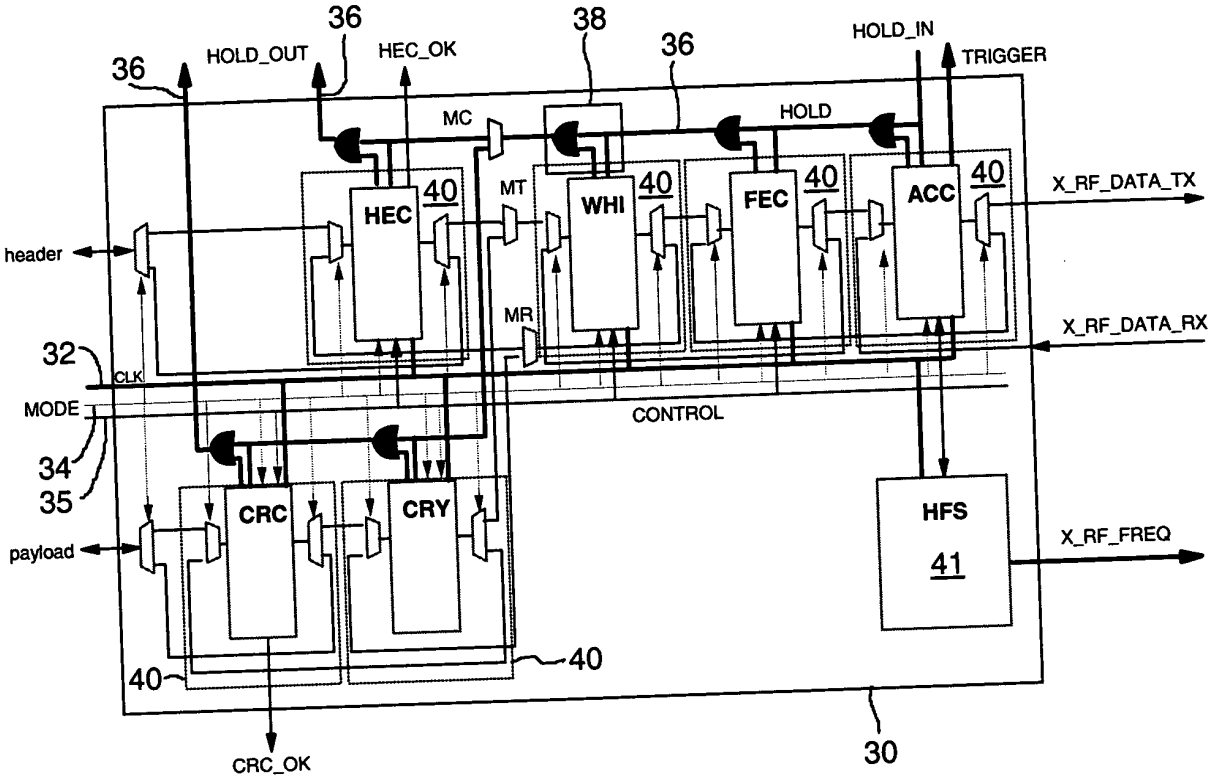
36
HOLD_OUT
36
HEC_OK
38
36
HOLD_IN
TRIGGER
MC
HOLD
HEC
40
MT
WHI
40
FEC
40
ACC
40
X_RF_DATA_TX
header
MR
X_RF_DATA_RX
32
CLK
MODE
CONTROL
34
35
CRC
CRY
HFS
41
X_RF_FREQ
payload
40
40
CRC_OK
30

Fig.3

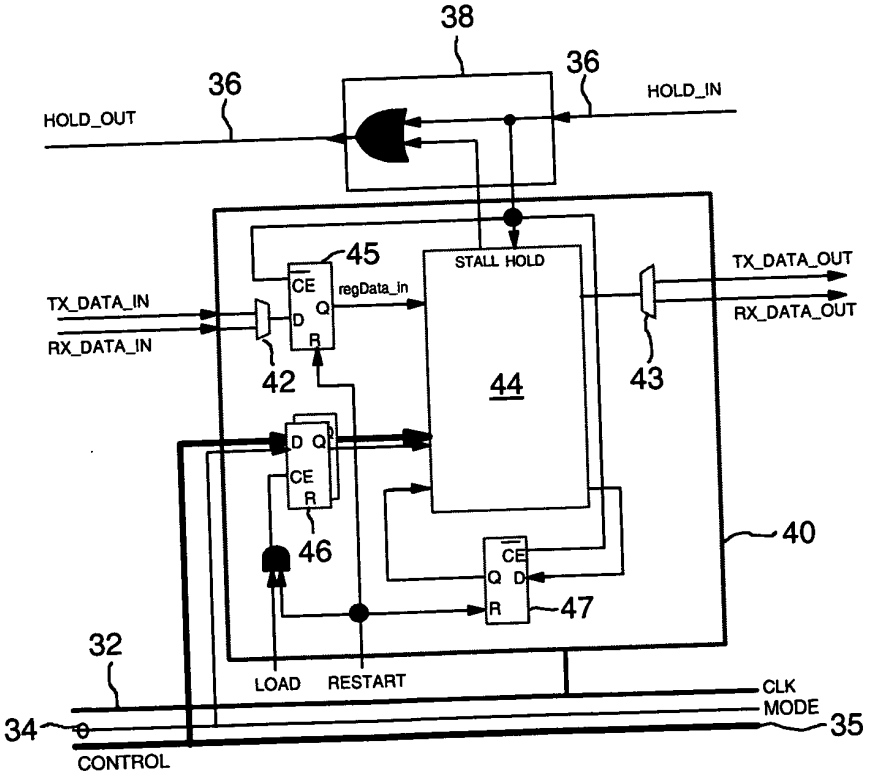
38
36
36
HOLD_OUT
HOLD_IN
45
STALL HOLD
TX_DATA_OUT
RX_DATA_OUT
TX_DATA_IN
RX_DATA_IN
regData_in
42
44
43
46
47
40
32
LOAD
RESTART
CLK
MODE
34
35
CONTROL

Fig.4

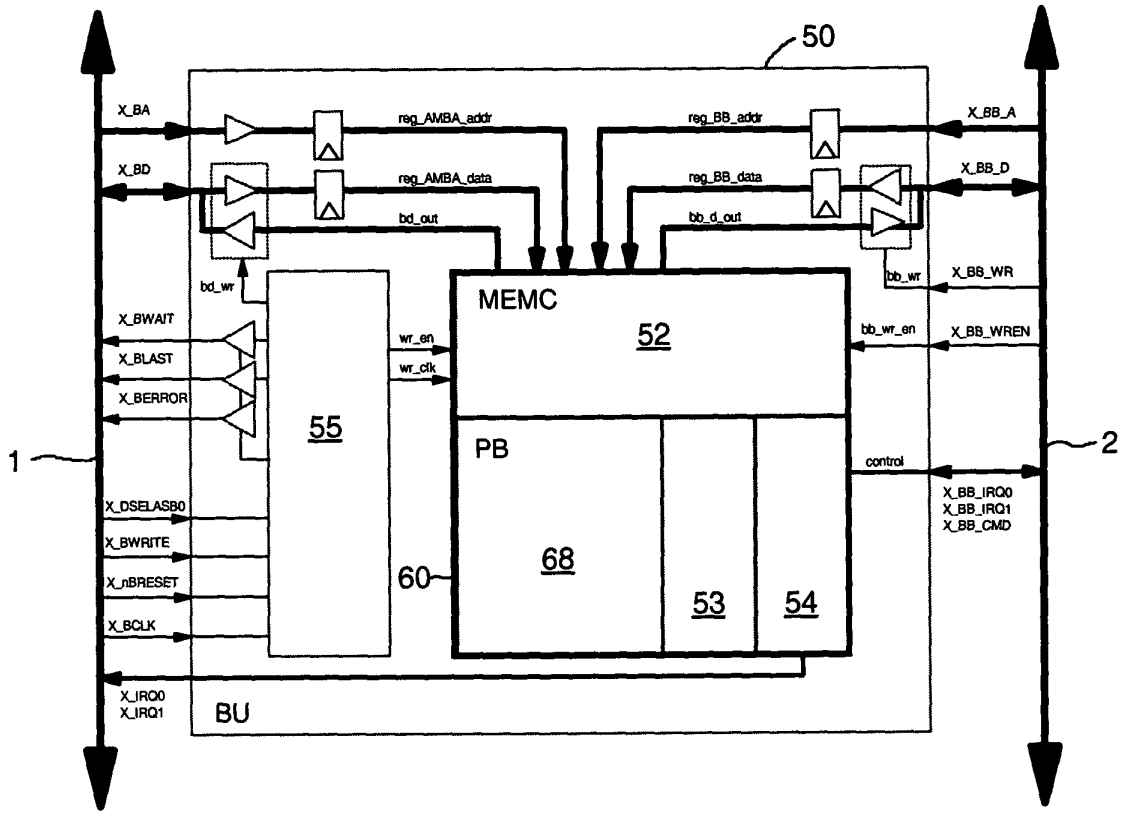
50
X_BA
X_BD
reg_AMBA_addr
reg_AMBA_data
bd_out
reg_BB_addr
reg_BB_data
bb_d_out
X_BB_A
X_BB_D
bb_wr
X_BB_WR
bd_wr
MEMC
52
X_BWAIT
X_BLAST
X_BERROR
wr_en
wr_clk
55
bb_wr_en
X_BB_WREN
PB
control
X_BB_IRQ0
X_BB_IRQ1
X_BB_CMD
1
2
X_DSELASB0
X_BWRITE
X_nBRESET
X_BCLK
60
68
53
54
X_IRQ0
X_IRQ1
BU

Fig. 5

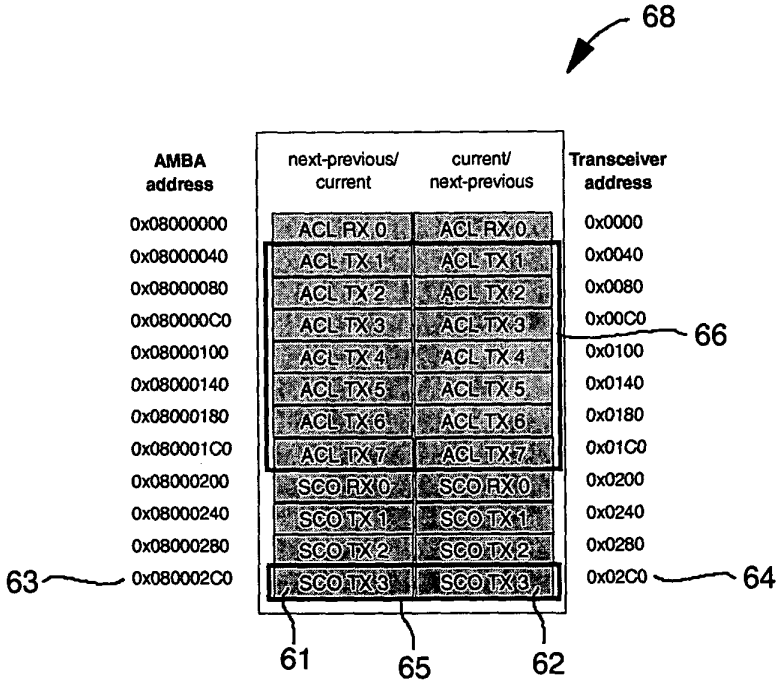
68
AMBA address
next-previous/ current
current/ next-previous
Transceiver address
0x08000000
0x08000040
0x08000080
0x080000C0
0x08000100
0x08000140
0x08000180
0x080001C0
0x08000200
0x08000240
0x08000280
0x080002C0
ACL RX 0
ACL TX 1
ACL TX 2
ACL TX 3
ACL TX 4
ACL TX 5
ACL TX 6
ACL TX 7
SCO RX 0
SCO TX 1
SCO TX 2
SCO TX 3
0x0000
0x0040
0x0080
0x00C0
0x0100
0x0140
0x0180
0x01C0
0x0200
0x0240
0x0280
0x02C0
66
63
64
61
65
62

Fig. 6

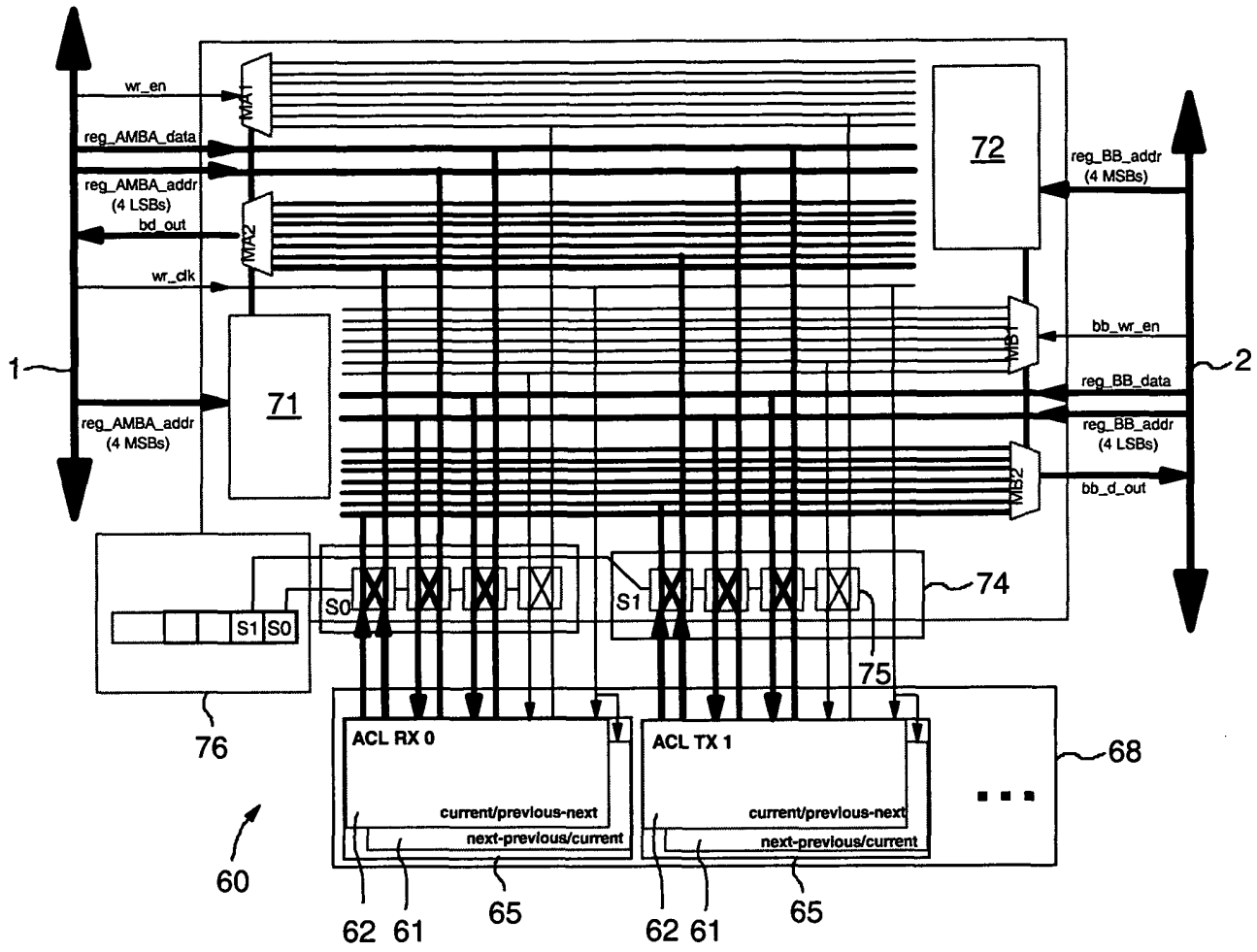
wr_en
reg_AMBA_data
reg_AMBA_addr
(4 LSBs)
bd_out
wr_clk
reg_AMBA_addr
(4 MSBs)
MA1
MA2
71
72
1
2
reg_BB_addr
(4 MSBs)
bb_wr_en
reg_BB_data
reg_BB_addr
(4 LSBs)
bb_d_out
MB1
MB2
S1
S0
74
75
76
ACL RX 0
ACL TX 1
current/previous-next
next-previous/current
68
60
62
61
65

Fig. 7

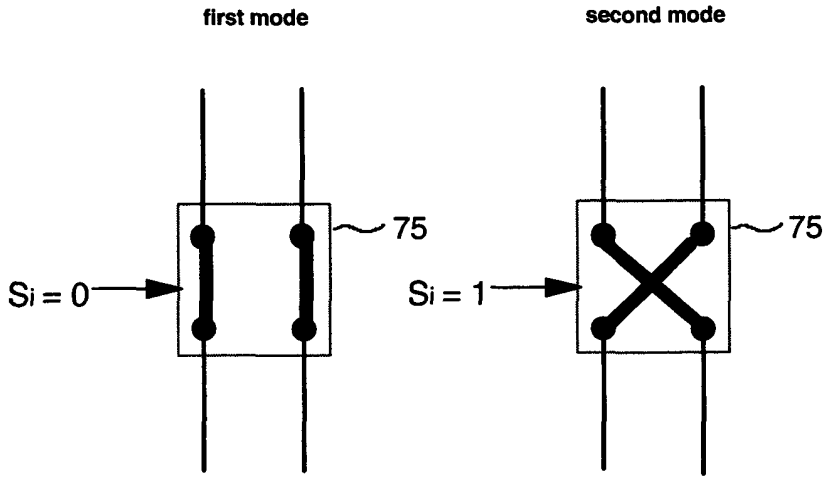
first mode
second mode
Si = 0
Si = 1
75

Fig. 8